REMARKS

This response is intended as a full and complete response to the Final Office Action dated December 9, 2005. In view of the amendments and the following discussion, the Applicants believe that all claims are in allowable form.

I. OBJECTIONS

a) Claims 29 and 34

The Examiner has continued the objection to claims 29 and 34 as containing limitations expressed in unclear language. The Examiner suggests that claims 28 and 29 are synonymous because the Examiner considers the terms "host workstation" and "testbench process" as being synonymous. The Applicants respectfully disagree.

In one embodiment of the invention, the testbench process is a process that is executed by the host workstation. As recited in Claim 27, when a service request occurs a signal is sent to the testbench process in the host workstation. Claims 28 and 29 recite what component, workstation generally or testbench process specifically, will service the signal. The use of the host workstation to service the signal (claim 28) is significantly of different scope than the recitation of using the specific testbench process to service the signal (claim 29). For example, claim 28 contemplates that the host workstation may suspend the operation until some other process (other than the testbench process) services the signal. Similarly, claim 29 specifically contemplates that the testbench process operates to service the signal. Since the scope of these claims is substantially different, claims 28 and 29 should not be considered synonymous. Furthermore, the applicants believe the recitation of the "testbench process" in claim 29 is clear as written and finds antecedent basis in the third line of claim 27. A similar argument can be made for claim 34. As such, the Applicants respectfully request that the objection to claims 29 and 34 be withdrawn.

II. CLAIM REJECTIONS

A. 35 U.S.C. §102(e) Claims 1-11, 13-15, 17-30, 32-34, and 36

Claims 1-11, 13-15, 17-30, 32-34, and 36 stand rejected as being anticipated by United States Patent No. 5,838,948 issued Nov. 17, 1998 to *Bunza* (hereinafter referred to as "*BU'948*"). This rejection is respectfully traversed.

The essence of the Applicants' invention is designing a behavioral processor into hardware, where the behavioral processor interacts with a host testbench processor. (See Applicants specification at page 204). The Applicants noted in response to the prior office action that the Applicants' behavioral processor is a hardware element (i.e., claim 1 recites " a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavioral level function"), while the *BU'948* reference discloses the uses of a hardware similator (i.e., a software program) to perform behavioral functions. The Examiner stated, in the present Office Action, that the rejected claims do not distinguish between hardware and software simulation. The Applicants disagree.

Claim 1 specifically recites that a "reprogrammable logic element" (Hardware) includes a behavioral level function. Such a use of a hardware element, as discussed in the Applicants' response to the prior Office Action is not taught by *BU'948*.

BU'948 teaches a system and method for simulation of target electronics ("user design") using a host workstation operating a process emulator and a hardware simulator coupled using a software kernel. A part of the target electronics is modeled using the process emulator ("reprogrammable logic") (see col. 9, lines 8-12 of *BU'948*), while "the hardware simulator and software kernel are both software components (see column 10, lines 2-64). The hardware simulator contains a process model shell emulating the actual pin connections of a target microprocessor (Fig. 6; col. 10, lines 20-26, 62-65). Clearly, *BU'948* defines a process emulator as a hardware element and a hardware simulator as a software element.

It is agreed as stated by the Examiner, that *BU'948* teaches an emulator that communicates with a simulator to perform hardware modeling. However, the

Applicants do not believe that *BU'948* teaches performing a behavioral level function in hardware and using a testbench call back process that responds to the behavioral level function. *BU'948* states, at column 9, lines 49-52, that the "use of unsynthesizable behavioral or high-level design representations, typical of early stages of design, are precluded by the use of hardware emulators." In the present office action, the Examiner states that this quote teaches that "unsynthesizable" behavioral representations are precluded from being synthesized in a hardware emulator. The Examiner further states that this clause "does not teach that synthesizable behavioral representations of the design are precluded from being synthesized in hardware emulator." Further, the Examiner states that it is inherent that "behavioral or high level representations can be synthesized into hardware emulator". The Applicant does not agree with this reasoning.

The Applicant does agree that *BU'948* specifically teaches that "unsynthesizable" behavioral level functions are precluded from being synthesized in a hardware emulator. At page 192, line 2-4 of the Applicants' specification, one embodiment of the invention specifically calls for the modeling of "normally non-synthesizable code elements" using hardware elements. As such, the present invention performs this particular aspect that *BU'948* states is not possible.

As for the inherency from the statement in *BU'948* of modelling synthesizable code into a hardware emulator, the Applicants do not agree.

It is established law that "inherency may not be established by possibilities or probabilities. The evidence must show that the inherency is necessary and inevitable". Interchemical Corp. v. Watson, 145 F. Supp. 179, 182, 111 USPQ 78, 79 (D.D.C. 1956), aff'd, 251 F. 2d 390, 116 USPQ 119 (D.C. Cir 1958). Because *BU'948* made a statement about "unsynthesizable functions" does not "necessarily and inevitably" teach that synthesizable behavioral functions can be modeled in hardware. *BU'948* is completely silent as to modelling of behavioral level functions in hardware. This silence does not infer that synthesizable behavioral functions can be modeled in hardware.

As for what *BU'948* does teach: at column 13, lines 55-60, *BU'948* does mention that the emulator (hardware) contains control circuitry and a control program that can

"identify conditions of the executing target program". These "conditions" are discussed and examples given that indicate that they are intended to prompt interaction with the simulator. At line 66, the control circuitry is identified as providing hardware capability to "detect events requiring interaction of the target microprocessor and the target circuitry". This event detection is not a behavioral level function nor is there any indication that the communication that is initiated by detecting an event is a testbench callback process. For comparison, note on pages 196-198 of the Applicants specification is a table of behaviors of the emulation that are controlled by the behavior processor. These are not event detections that initiate communications with a simulation, these are commands that control the behavior of the emulation. *BU'948* simply does not teach generating behavior level functions within the emulator hardware.

In contrast to what is taught by *BU'948*, the applicants' claim 1 specifically recites "a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function".

BU'948 is devoid of any such teaching. Furthermore, *BU'948* is also devoid of any teaching of "a testbench call back process for responding to the behavior level function in the reprogrammable logic element", as also recited in applicants' claim 1. The Examiner cites col. 12, lines 63-67 and col. 13, lines 1-6, 8-13 as teaching a "testbench process". However, these portions teach that the emulator communicates with the simulator through a translator. There is no teaching of a testbench call back process that responds to a behavioral level function by sending a signal to the host testbench process. The Applicants do not find any indication that any signal is communicated to the host workstation that could be construed as a signal to a host testbench process.

Independent claims 13, 27, and 32 also recite similar subject matter as recited in claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir.

1984) (emphasis added). Since *BU'948* lacks any disclosure of a behavior level function being modeled in a reprogrammable logic element nor a testbench call back process, the applicants contend that claims 1, 13, 27, and 32 are patentable over *BU'948* and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

Furthermore, claims 2-11, 14-15, 17-20, 22-23, 25-26, 28-30, 33-34, and 36 depend, either directly or indirectly, from claims 1, 13, 27, and 32 and recite additional features therefor. Thus, the applicants submit that independent claims 1, 13, 27, and 32 and claims 2-11, 14-15, 17-20, 22-23, 25-26, 28-30, 33-34, and 36 depending therefrom are patentable over *BU'948*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

B. 35 U.S.C. §103(a) Claims 4, 16, 31, and 35

Claims 4, 16, 31, and 35 stand rejected as being unpatentable over *BU'948* in view of IEEE Std 1364-1995 "IEEE Standard Hardware Description Language based on the Verilog® Hardware Description Language" (hereinafter referred to as "*IEEE1364*").

Independent claims 1, 13, 27, and 32, as discussed above, recite a reprogrammable logic element that models a behavior function (or behavioral portion) of a user design. *BU'948* does not teach or suggest modeling a behavior function or behavioral portion of a user design in a reprogrammable logic element nor does *BU'948* teach the use of a testbench call back process.

IEEE1364 teaches conditional expression for state dependent paths, but is devoid of any teaching or suggestion of using a reprogrammable logic element to model a behavioral function of a user design. Nor is there any disclosure of using a testbench call back process that responds to the behavioral function. Since the same elements are lacking from both *BU'948 and IEEE1364*, no permissible combination of these references teaches or suggests the applicants' invention as recited in independent claims, 1, 13, 27, and 32.

Claims 4, 16, 31, and 35 depend, either directly or indirectly, from claims 1, 13, 27, and 32 and recite additional features therefor. Since a combination of *BU'948* and

IEEE1364 would not produce applicants' invention as recited in claims 1, 13, 27, and 32, dependent claims 4, 16, 31, and 35 are also not obvious and are allowable.

Thus, the applicants submit that claims 4, 16, 31, and 35 are patentable over *BU'948* in view of *IEEE1364*. Accordingly, the applicants respectfully request the rejection be withdrawn.

C. 35 U.S.C. §103(a) Claims 12 and 37

Claims 12 and 37 stand rejected as being unpatentable over *BU'948* in view of an article "A 145MHz User-Programmable Gate Array" by Eduardo do Valle Simoes et al. (IEEE Transactions on Computers, 1995, pp. 226-232, hereinafter referred to as "*ED1995*").

Independent claims 1 and 32, as discussed above, recite a reprogrammable logic element that models a behavior function or behavioral portion of a user design. *BU'948* does not teach or suggest modeling a behavioral function or portion in a reprogrammable logic element nor does *BU'948* teach a testbench call back process.

ED1995 teaches conditional expression for state dependent paths, but is devoid of any teaching or suggestion of using a reprogrammable logic element to model a behavioral function of a user design. Nor is there any disclosure of using a testbench call back process that responds to the behavioral function. Since the same elements are lacking from both *BU'948 and ED1995*, no permissible combination of these references teaches or suggests the applicants' invention as recited in independent claims 1 and 32.

Claims 12 and 37 depend, either directly or indirectly, from claims 1 and 32 and recite additional features therefor. Since the combination of *BU'948* and *ED1995* would not produce Applicants' invention as recited in claims 1 and 32, dependent claims 12 and 37 are also not obvious and are allowable.

Thus, the applicants submit that claims 12 and 37 are patentable over *BU'948* in view of *ED1995*. Accordingly, the applicants respectfully request the rejection be withdrawn.

CONCLUSION

Thus, the applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Raymond R. Moser, Jr. at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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